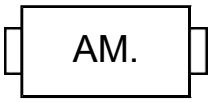
Features

- 3700W Peak pulse power per line (tP =8/20μs)
- SOD-123FL package
- Response time is typically < 1 ns
- Protect one I/O or power line
- Low clamping Voltage
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD)±30KV(air), ±30KV(contact); IEC 61000-4-4 (EFT) 40A (5/50ns)
- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260℃
- Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil

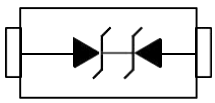
Applications

- Cell phone handsets and accessories
- Personal digital assistants (PDA's)
- Notebooks, desktops, and servers
- Portable instrumentation
- Cordless phones
- Digital cameras
- Peripherals MP3 players

Circuit Diagram & Pin Configuration:



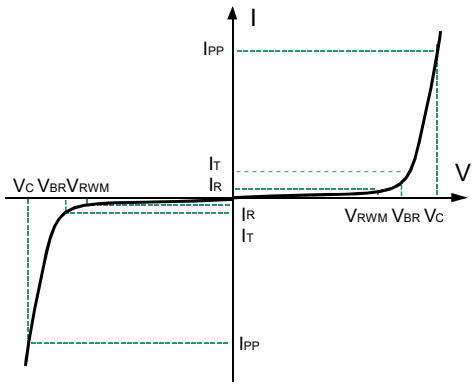
SOD-123FL



DEVICE MARKING AND ORDERING INFORMATION			
Device	**Package**	Marking	**Shipping**
ESD1D7VB1S372P	SOD-123FL	AM	3000/Tape&Reel

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance



Electrical characteristics per line@25℃(unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				7	V
Breakdown Voltage	V_{BR}	I_t =1mA		7.8		V
Reverse Leakage Current	I_R	V_{RWM} =7V			200	μA
Clamping Voltage	V_C	I_{PP}=185A t_P = 8/20μs		19	22	V
Junction Capacitance	C_j	V_R=0V f =1MHz		520	550	pF

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_P = 8/20μS)	P_{pp}	3700	W
Lead Soldering Temperature	T_L	260 (10 sec)	℃
Operating Temperature	T_J	-55 to +150	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Typical Characteristics

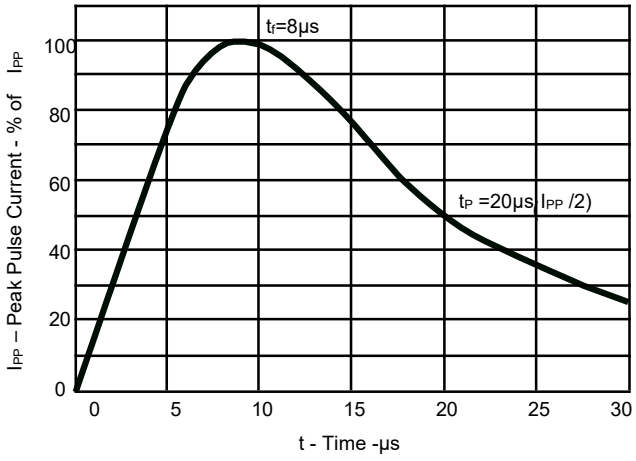


Fig 1.Pulse Waveform

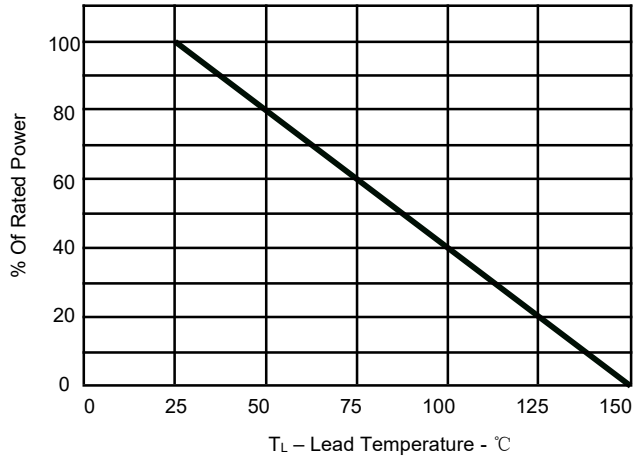


Fig 2.Power Derating Curve

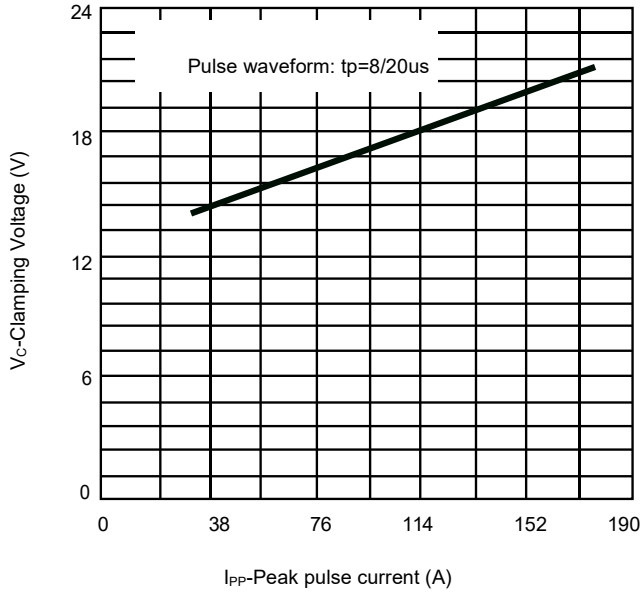


Fig 3. Clamping voltage vs. Peak pulse current

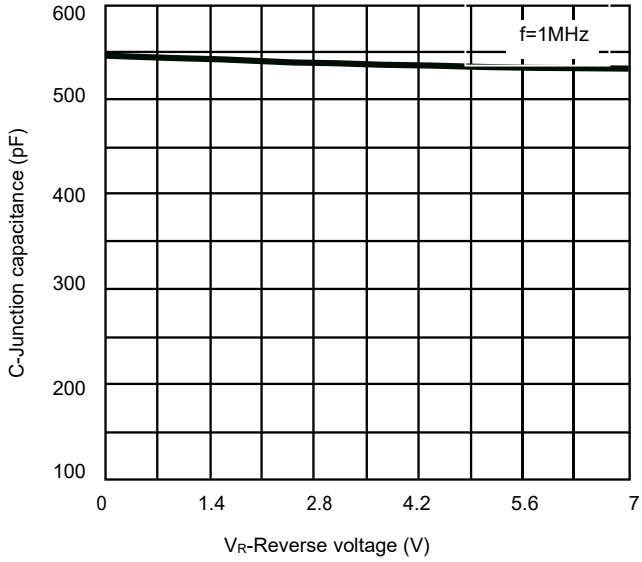


Fig 4. Capacitance vs. Reveres voltage

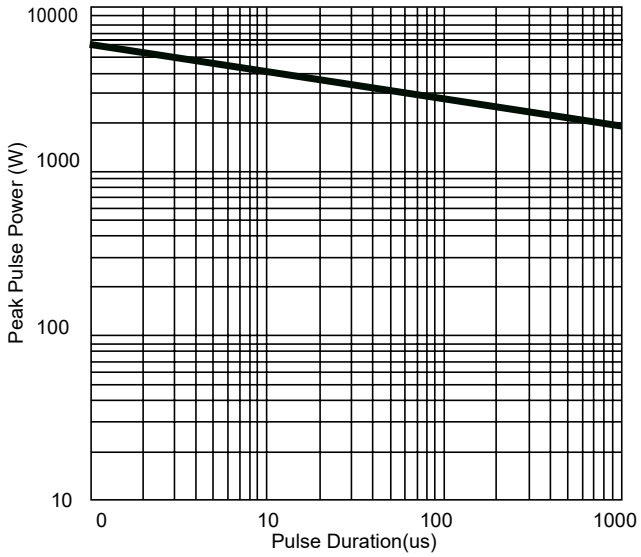
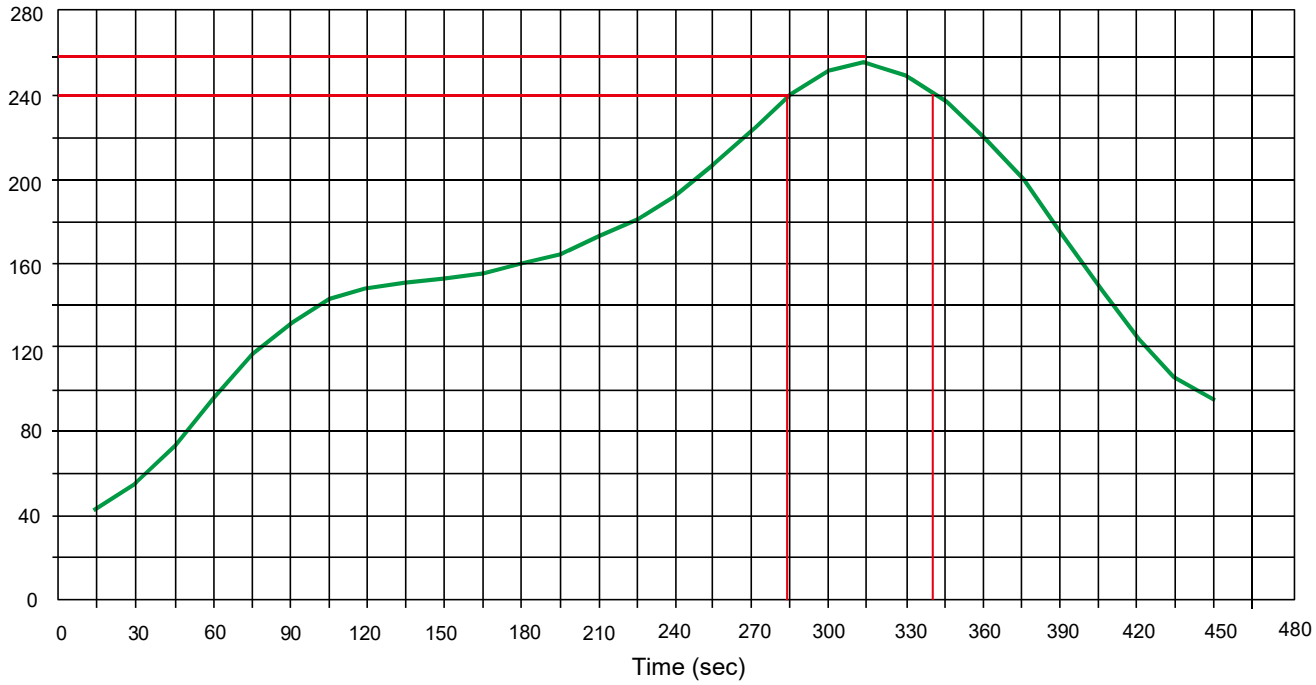


Fig 5. Non Repetitive Peak Pulse Power vs. Pulse time

Solder Reflow Recommendation

Peak Temp=257℃, Ramp Rate=0.802deg. ℃/sec

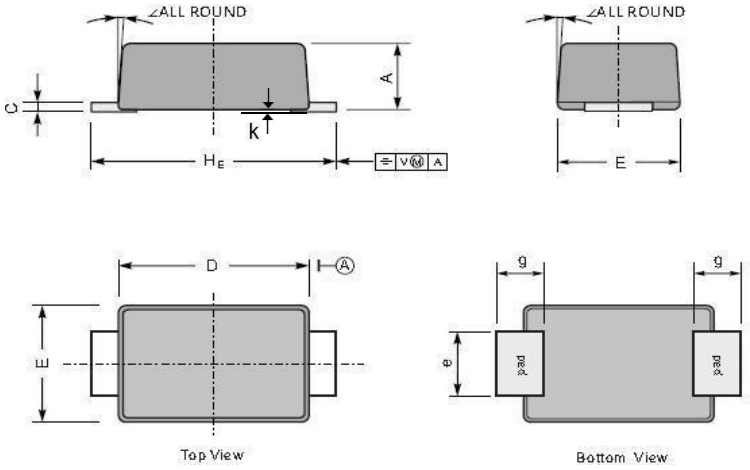


PCB Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

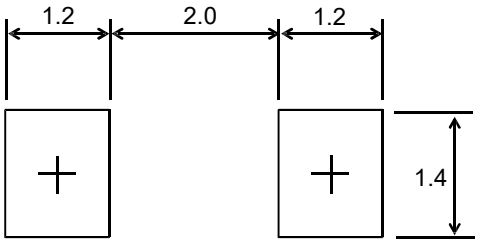
- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

Product dimension (SOD-123FL)



Unit:mm

Dim	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.031	0.047	0.80	1.20
C	0.002	0.010	0.05	0.25
H_E	0.138	0.154	3.50	3.90
E	0.061	0.077	1.55	1.95
D	0.098	0.114	2.50	2.90
g	0.020	0.043	0.50	1.10
e	0.024	0.039	0.60	1.00
k	0.004		0.10	
∠	7°			



Suggested PCB Layout Unit:mm